Design and Analyses of a PWM based Seven Level Cascade-Combination Inverter

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Abstract

Multilevel Inverters has big placement advantages in Power Electronics and its application can be mentioned to FACTS tools such as UPFC – D-STATCOM. Therefore, nowadays Multilevel Inverters have created vast field's research and researchers are trying to present appropriate structures with fewer keys and greater advantages. The main advantages of Multilevel Inverters mentioned are low-key voltage stress and low harmonic content of the output voltage. Multilevel Inverters, having many advantages, can be referred to have low volume, low EMI, low losses and high efficiency. In this study, all equations dominating the circuit have been investigated and main and effective parameters have been identified in suggested Invertors and this method has been extended for use in n levels Invertors. Then it has investigated the changes possibility in the Invertors' structure aiming to reduce dc voltage and to increase the number of output voltage levels. The results of simulations have emphasized the suggested structures.

Keywords: Inverter, Cascade hybrid, Pulse with Modulation, Seven Levels

1- Introduction

Voltage Inverters are the most fundamental power electronics equipment and nowadays with the advances in power semiconductor technology, these Inverters are used in industry sectors and robots [1, 17-18]. Foundation of multilevel inverters' work is to convert the DC input voltage to AC output voltage with desired frequency and range. The provided voltage, having been provided by renewable energy, is often kind of DC and the output voltage must be converted into AC voltage with desired range for exploiting them. In this process the electronic convertor has the great importance such as being chopper, inverter and power invertors and plays an essential role. By attending to the variation of these resources, there are types of invertors' structure that basically have used high voltage sources in construction. This issue caused the achieved Inverter efficiency to be reduced and its weight and volume and electromagnetic

interference be increased and also construction costs have gone to high, and it is not appropriate for small-scale applications such as electronic systems. The normal multilevel inventors have many semiconductor devices control, reducing reliability. and increasing costs [4]. Therefore, an inventor must be designed, having simpler construction and more economical and being appropriate for special application and also has some conventional multilevel inverters' advantages. The first advantage of multilevel invertor is higher output quality [5], lower harmonic component [6], better electromagnetic compatibility and lower switching losses. The most general structures are H-bridge cascade invertor and its derivatives [8] (Multi-level inverter with chopper diode, capacitor-float multilevel inverters). The main benefit of conventional structures is further reduction of switching equipment compared to other specimens. However, a large number of needed switching equipment is equal to (k-1), where k is the number of levels. Therefore, according to the number of direct level, almost the switching equipment will be doubled and consequently increasing this equipment will be along with increasing circuit complexity and reducing efficiency ensures. In present research, the design of the new seven-level cascade-components inverter will be presented by Pulse Width Modulation methods.

2- Pulse Width Modulation

Pulse Width Modulation (PMW) is a more effective way to provide desired value of power between its maximum and minimum [11]. A simple power switch passes resource on when voltage is turned; PMW has been implemented by electronic power switches. Figure 1 shows the ratio between the sine reference signal and the triangular signal is used to generate PWM signal. PMW output signal is 1 when $V_{ctrl} > V_{tri}$ and it is 0 when $Vctrl < Vtri$ and PMW signal bandwidth can be defined in the form of equation [12-15].

$$0 \le A_{ctrl} \le 1$$
$$T_{PWM} = A_{crrl} \times T_{tri} \qquad (1)$$

Where, A_{ctrl}, is signal range control, T_{PWM}, PMW signal bandwidth, T_{tri}, alternation period of triangular signal.

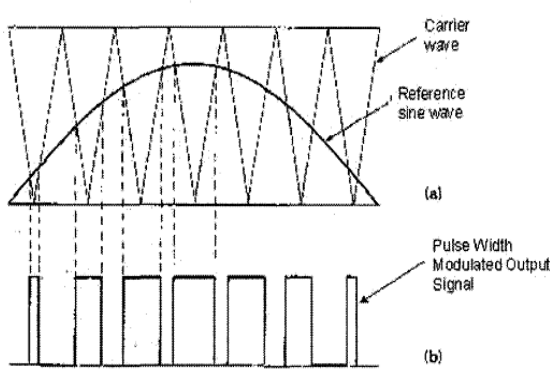

Fig. 1. Sinusoidal pulse width modulation [16]

3- Suggested Structure

In this study, it has been suggested on the structure of a new inverter, shown in fig. 1. This structure includes a leg of H-Bridge with key Bidirectional, obviously reducing, the complexity of the power circuit. New

inverter structure shown in the block diagram, has suggested a significant improvement and amendment for using fewer components and reducing the complexity of the circuit layout, compared to

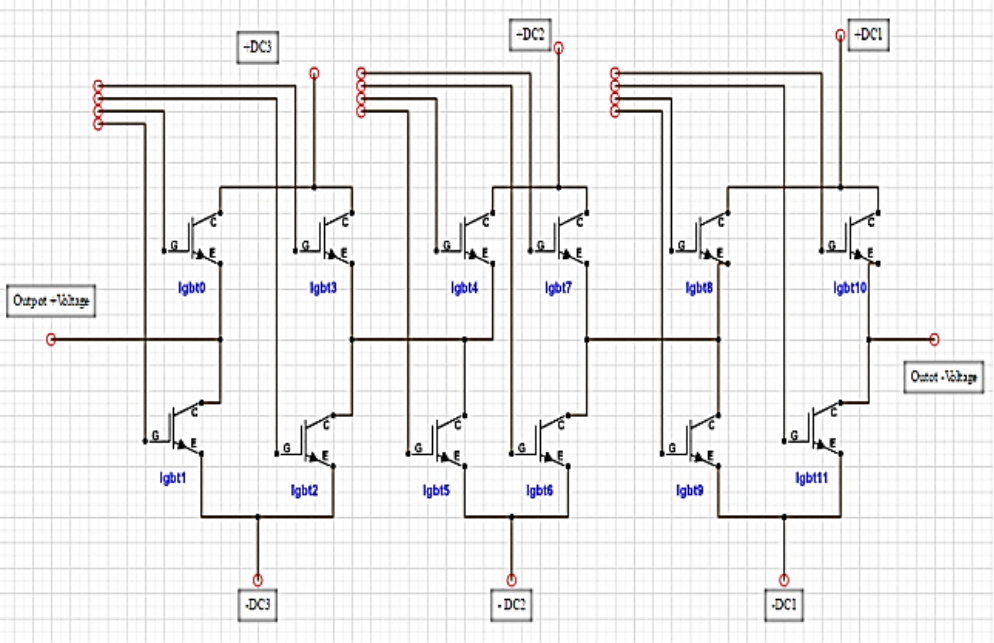

Fig. 2. the proposed basic 7-level inverter structure

the five-level converters provided in inverters with floating capacitor and inverters with chopper diode. The Combined Invertors are to present semiconductor switches at different frequencies and converters symmetric, asymmetric transducers with DC sources. Figure 2 has suggested the basic 7-level inverter structure. This invertor, having 3 dc voltage source and 12, IGBT is designed for Ohmic loads. When T_1 and T_4 keys simultaneously are turned off, output voltage is equal toV_1, and when T_3 and T_4 keys simultaneously are turned on, the output voltage is equal to zero. Similarly, other voltage levels are accessible as presented in Table 1. In drawing this figure, it is assumed$V_1 < V_2 < V_3$. As this figure shows the basic proposed structure is able to produce only positive and zero voltage levels. The following general plan of simulation block diagram is provided below. Figure 3-2 shows the structure of the proposed inverter as seen in the mentioned simulation, having several sub-systems presented in Figure 3-1, related to the inverter. In table 1, it is provided how keying is done in the proposed inverter. It has been presented in the new PWM modulation method to produce switching signals, having three references signal with the carrier signal. References' signal, having same frequency and ratio and the offset value, is equal to the range of carrier signal.

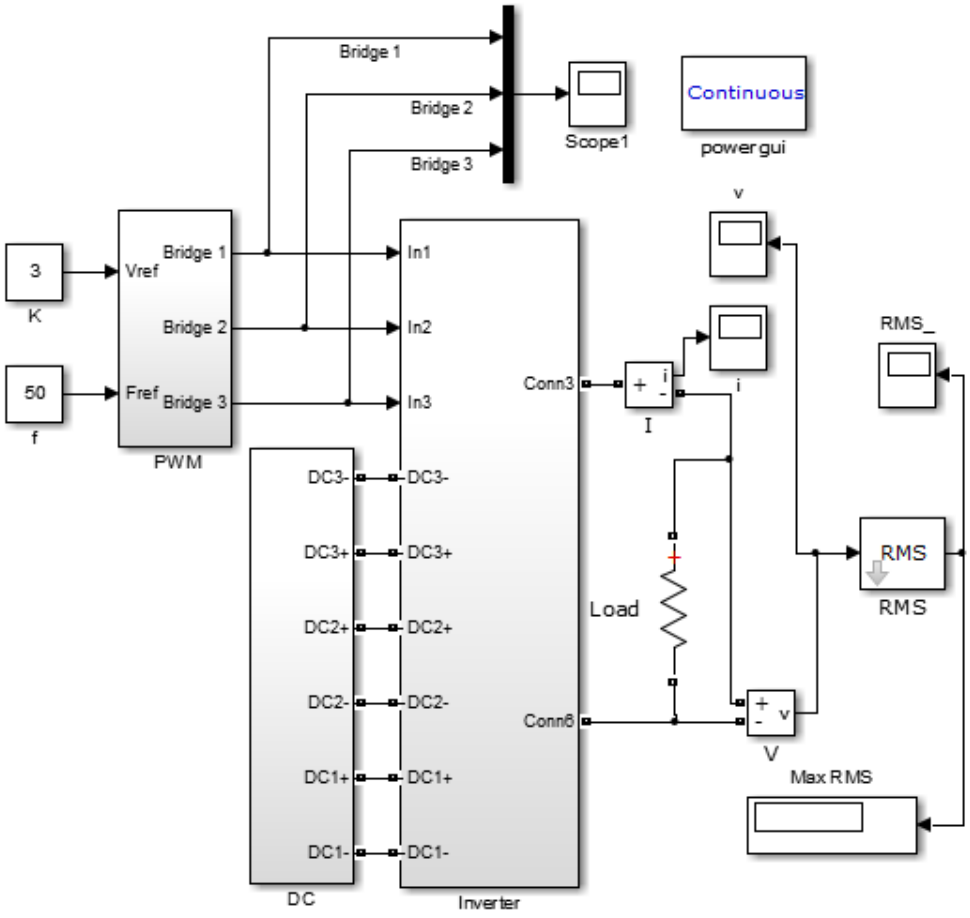

Fig. 3. Block diagram of the overall structure of the proposed inverter

In other words, the reference signal is comparable with the carrier signal. If reference signal 1, being more than carrier signal, the reference signal 2 will be compared to when peak of the range will be more than the carrier signal. Then, reference signal 3 has been implemented and can be compared to when it goes to zero. When reference signal 3 is zero, reference signal 2 is implemented to get to zero. Then, reference signal 1 is compared to carrier signal.

Table 1: Switching in the proposed inverter

V_o	T1	T2	T3	T4	T5	T6
V_{dc}	On	Off	Off	On	Off	Off
$2V_{dc/3}$	Off	Off	Off	On	On	Off
$V_{dc/3}$	Off	Off	Off	On	Off	On
o	Off	Off	On	On	Off	Off
$-V_{dc/3}$	Off	On	Off	Off	On	Off
$-2V_{dc/3}$	Off	On	Off	Off	Off	On
$-V_{dc}$	Off	On	On	Off	Off	Off

4- RESULTS AND DISCUSSION

4-1- Signal Production

As also shown in the previous section, producing simulation signal has been implemented in a way that it is able to produce a different kind of signal in order to provide different levels of flow by inverter. In figure 4 the produced signal has been presented for each of the three existence bridges in the inverter. By considering that signals produced by the merger of Mentioned diagram graph have been busy, each graph is separately presented. The output frequency is tuned in 50Hz. And Load profile is ($R = 100\Omega$. Dc resources' voltage has been selected as $(V_1 = 25, V_2 = 75, V_3 = 225)$.

It is necessary that other switches are employed to change the value of K voltage levels and based on the type of the required level, they are launched as number of intended switch.

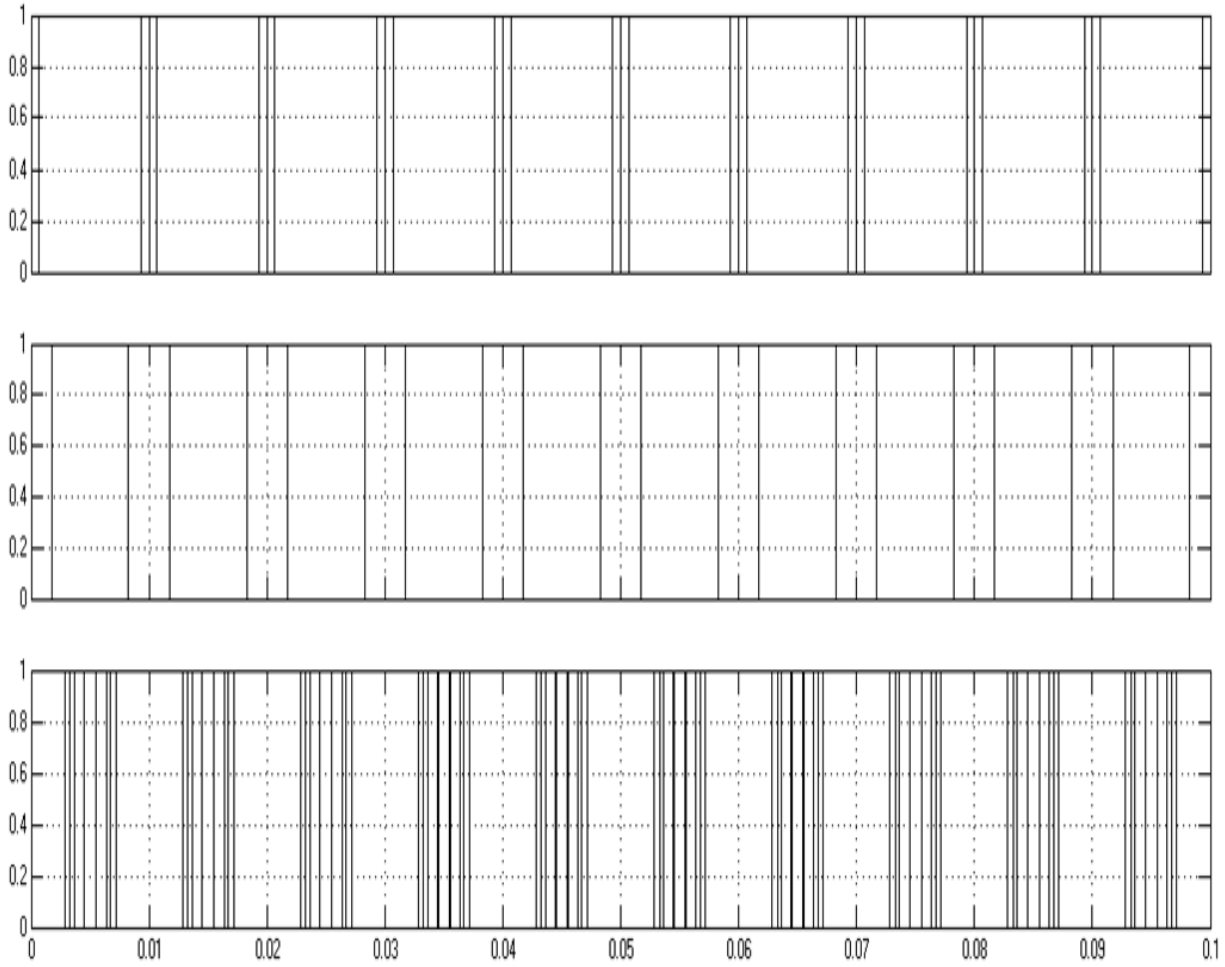

Fig. 4. Signal produced by switches 1, 2, and 3

4-2- Invertor Output Current

The control signal has been produced and output voltage has been calculated by using MATLAB Simulink Toolbox. The output voltage can be controlled by modulation index and output frequency by adjusting the frequency. The simulation results shown in Figure 5, are proposed Inverter 7-level cascade.

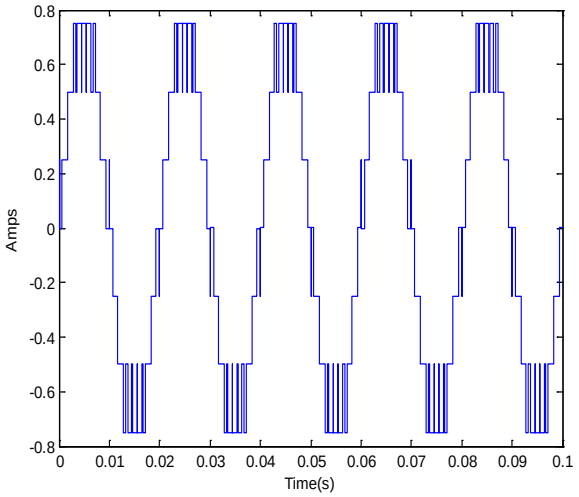

Fig. 5. Current produced by the 7-level inverter

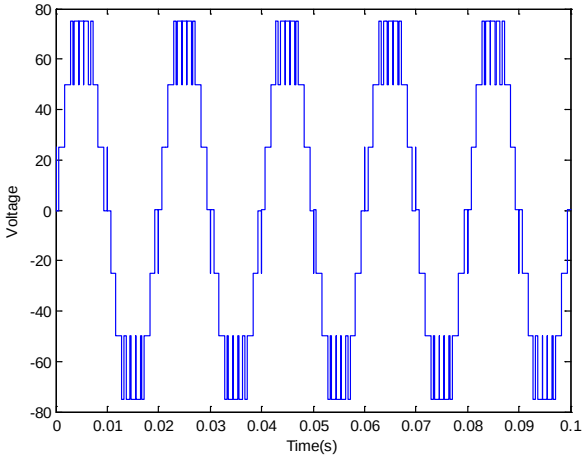

Fig. 6. The voltage produced in 7-level inverter

In figure 5 produced Current has been presented by the 7-level inverter. Accordingly, the proposed form can be seen as the current is located in the period of (+0.8, -0.8). Voltage inverter is provided in Figure 6, having clearly necessary coordination with the stream and also the produced Current has 7-level. Descriptions of each of the voltages in 7-level mode are shown in Figure. Furthermore, correct root mean square has been used in order to determine the error existing in voltage of the RMS block or to calculate the diagram presented in Figure 8.

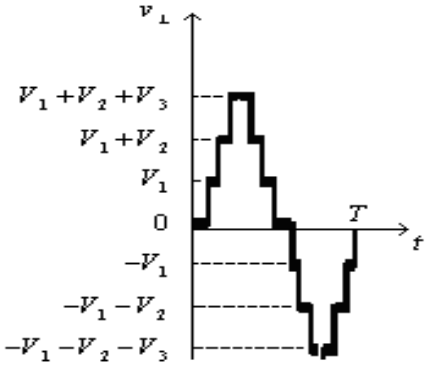

Fig. 7. Describing the current levels produced in the 7-level inverter

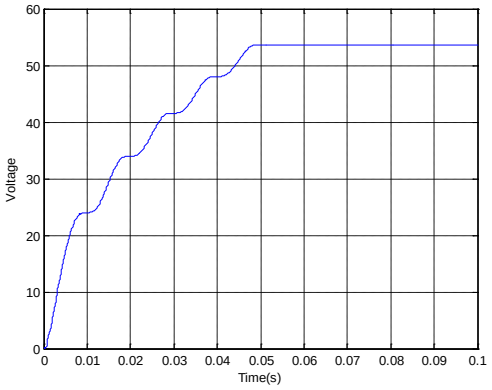

Fig. 8. The RMS value of current produced in the 7-level inverter

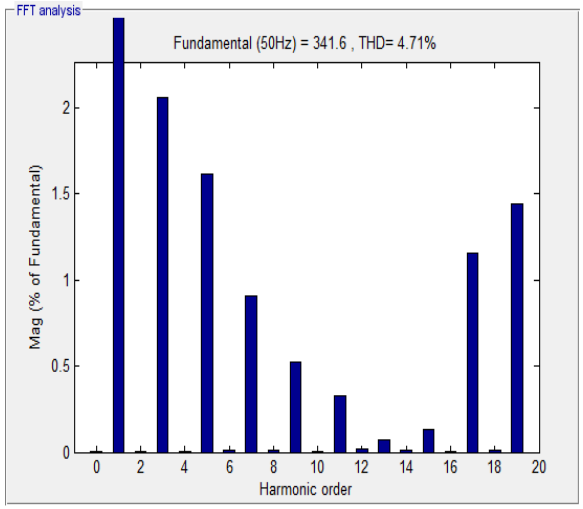

Fig. 9. THD output voltage and current at the 7-level inverter

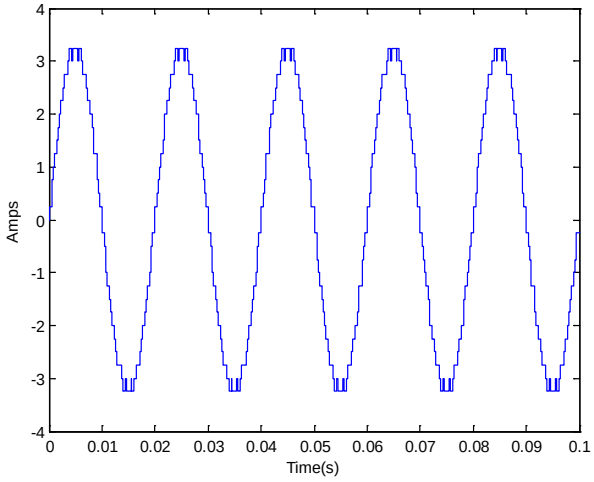

Fig. 10.the Flow produced in the 27-level inverter

THD value on the 7-level is equal to 4.71 %. As mentioned earlier, such a simulation is conducted that is able to provide different levels of voltage. Therefore, the following modes of 9, 11, 13 and 27-level are provided, which reflect high simulated structure performances.

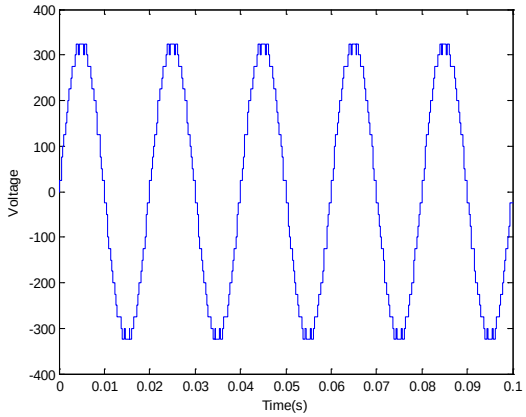

Fig. 11. the voltage produced in the 27-level inverter

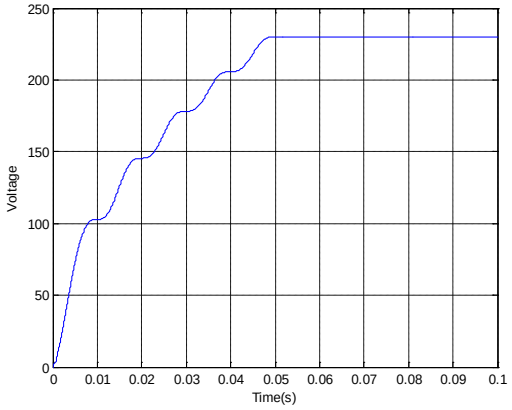

Fig. 12. the RMS value produced in the 27-level inverter

The only requirement change is to prepare each of Mentioned levels of K (number of levels= 2K+1).). Voltages with 100, 120, 150 and 325 volts are generated by using this inverter. It should be noted that the output frequency and Load profile and dc voltage resources are considered constant. Figures 10, 11, 12 and 13, respectively, show current, voltage, RMS and THD produced at 27-level inverter. Table 3 proposes the comparison between different voltage levels provided by the inverter

Table 3: Total comparison of designed inverter

Level Number	Voltage	Current	RMS	THD
7	75	0.75	753.6	**14.7**
9	100	1	71.68	**4.69**
11	125	1.25	78.6	**4.65**
13	150	1.5	106	**5.3**
27	325	3.25	230	**4.69**

4- CONCLUSIONS

In this study, multilevel inverters (7, 9, 13 and 27) have been designed with input dc resources by unequal plans. Suggested inverter performance was evaluated by simulation. This structure can produce the number of voltage levels with fewer parts in comparison with conventional structures. The suggested inverter will be available by utilizing DC voltages by different voltage levels. Suggested inverters have advantages such as volume reduction, losses reduction, cost reduction and improving efficiency.

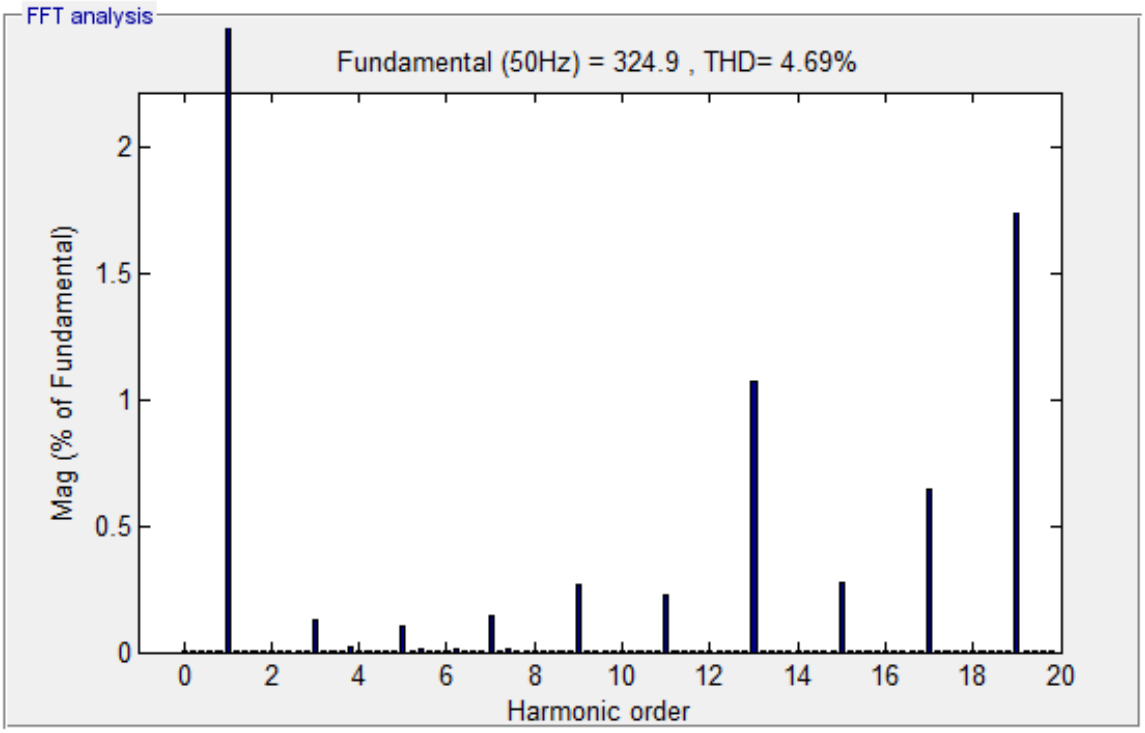

Fig. 13 . THD in 27-level invertor

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