

Analysis and Simulation of an Augmented DC-DC Converter With the Ability to Remove the Flow of Input Stream

Faezeh Ebrahimzadeh^{1*}, Ebrahim Babaei²

¹Department of Electrical Engineering, Ahar Branch, Islamic Azad University, Ahar, Iran b Faculty of Electrical and

²Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz ,iran

F_ebrahimzadeh123@yahoo.com

Abstract:

In this article a boost dc-dc converter with the ability to remove the input current ripple is given for specific work cycle. Ability to remove the input current ripple in this structure is obtained without increasing the number of elements compared to other structures. In addition, the converter provided without the need for a large cycle of work or boost transformers produced high voltage gain without utilizing high values of duty cycle or boosting transformers. These features make the converter provided for the transfer of low voltage power sources, such as renewable resources. The converter operation has been investigated in the working modes and the relations related to this converter have been calculated. Ultimately the structure is provided in the PSCAD software and simulation results are presented to validate the performance and relationships obtained for this structure.

Keywords: zero current ripple, dc-dc converters, power conversion, pulsewidth modulation (PWM)

1. Introduction.

Given that the voltage range generated by renewable energy sources is low, a boost converter with a high voltage gain is required to connect the low voltage output from the renewable source to the inverter. Another important reason for the use of a converter in renewable energy applications (for example, in fuel cells) is the passage of a continuous current with a minimum of ripples. Consequently, converters with mentioned two characteristics can have many applications in renewable energy systems. Theoretically, a typical boost converter can generation unlimited voltage gain for 100% Work cycle. But in practice, the leakage resistance found in the charge loop of the inductor limits the voltage of the

converter [1]. Therefore, a boost converter is not used when the gain of a voltage greater than 4 is required. A common method for solving this problem is the use of small reactive elements along with an increase in the switching frequency of the converter for an acceptable amount of the ripple [2]. Semiconductors limit the very small or very large operating frequency of the switching frequency.

A common way to solve this problem is to use a transformer to increase the voltage without using Very large voltages working cycle.[3-4]Other solutions are the basis of the use of a switched capacitor with a combination of features of converters with coupling inductors with voltage amplifiers or provided SC amplifiers [5 - 7]. converters

without Switched inductor couplers have been used for low power applications, but at high power levels, ordinary converters is preferred due to the low number of semiconductors, the presence of a multiplier throughput between the capacitors and the high frequency switching frequency .the multi-stage SCcircuitsare provided to increase Voltage gain[8 -10]. in power converters with the transformer, the switching frequency voltage is limited for gain increase, because when the switching frequency is high, the transformer's loss increases. In the reference [11] the switching capacitors are supplied with full intermittent charge and reference [12] Modulation PWM converter is presented for voltage regulation.

The CCI circuits with the SC function capability is not used to regulate the voltage due to the negative effects of this on. However, the CCI combination of a circuit, PWM, improves the efficiency of both converters with a SC controller. In short, high voltage gain converters that do not require transformers, coupling inductors, and very high cycle cycles are very desirable for low voltage power supplies. Another important challenge in the low-power renewable energy systems is the low input current. The common method for reducing of input current ripple is the use of large inductors. But large inductors are heavier and cost big in size and cost. In addition, a large inductor reduces the transient response rate. In this paper, DC-DC converter is presented as an boost converter that has two important DC features : 1) to remove the input ripple in the output of the converter is inserted two inductors , 2) in the output of

converter circuit is inserted a capacitor which is switched on to increase the voltage gain. By placing a small resonant inductor in the switching capacitor class, the maximum current due to the switching process is improved and thus preventing the high impact currents. Unlike the transducers presented in references [5-7] or coupling inductors, it is possible to use power semiconductors with fast switching in the converter. Unlike the reference [11], the converter provided in this article removes the input current ripple. Additionally, the converter combines a CCI-SC circuit with a boost converter, and the voltage regulating is done without reducing the converter's output gain.

2. The Structure of The Proposed Converter

The proposed Converter power circuit is shown in fig.1a. BY considering fig.1a the proposed converter has two transistors S2 and S1, three diode D3 and D2, D1, three capacitors C1, C3 and C2, two inductors L2 and L1 for storing energy and an small inductor, L3 to limit the current of D3. in practical, the size of L3 is equal to 1/100 of and L2 and 1/50 of and L1. due to the small size of that, the size of the inductor does not require for L3 a value of 1/50, in result the inductance of that determine based on CCI between C3 and C2. transistors turn on in complacently form. The equivalent circuit of the proposed converter is shown for the operating modes in the form (1-B) and (1c). when the key S1 is turned on and the key S2 is turned off, the circuit is equivalent to the fig 1.c .

In this mode, D1 is reverse bias and is cut to C3 voltage. D3 is also reverse bias mode and is cut to C3 voltage. the current of the L2 passes from D2 due to turn off key S2. fig.2 shows of the input current, the current of L2, the current of L1, the current of D3 the trigger pulses of S1 and S2 switches. When the S1 is turn on according to the fig 1b the current flowing from the inductor L1 increases with equal to slope of V_i/L_1 and the current of L2 is discharged with equal to slope of $V_i - V_{C2}/L_2$. When S2 is turn on, S1 goes to turn off mode, and the equivalent circuit of this mode is activated according to the fig 1b.

According to the fig 1b , the current of L1 is discharged with equal to slope of $V_i - V_{C1}/L_1$ and the current of L2 is charged with equal to slope of V_i/L_2 . When the S2 is turn on the capacitors C1 and C2 are connected in parallel, and a type of SC mode is created and so a small inductor L3 is required to limit the maximum current passing through the loop of the C1 ,C3 and L3 . The current waveform of L3 is shown in fig 2. the input current of converter is equal with the sum of L1 and L2 output currents. since the L2 and L1 are both charged and discharged complementally, these two inductors can be designed such that the input current ripple for a given value, for the working cycle is equal to zero. the current waveforms shown in fig 2 are for zero input current ripple in the working cycle $D = 75\%$, In this case, two inductors are charged with equal voltage, and $L_2 = 3L_1$ is.

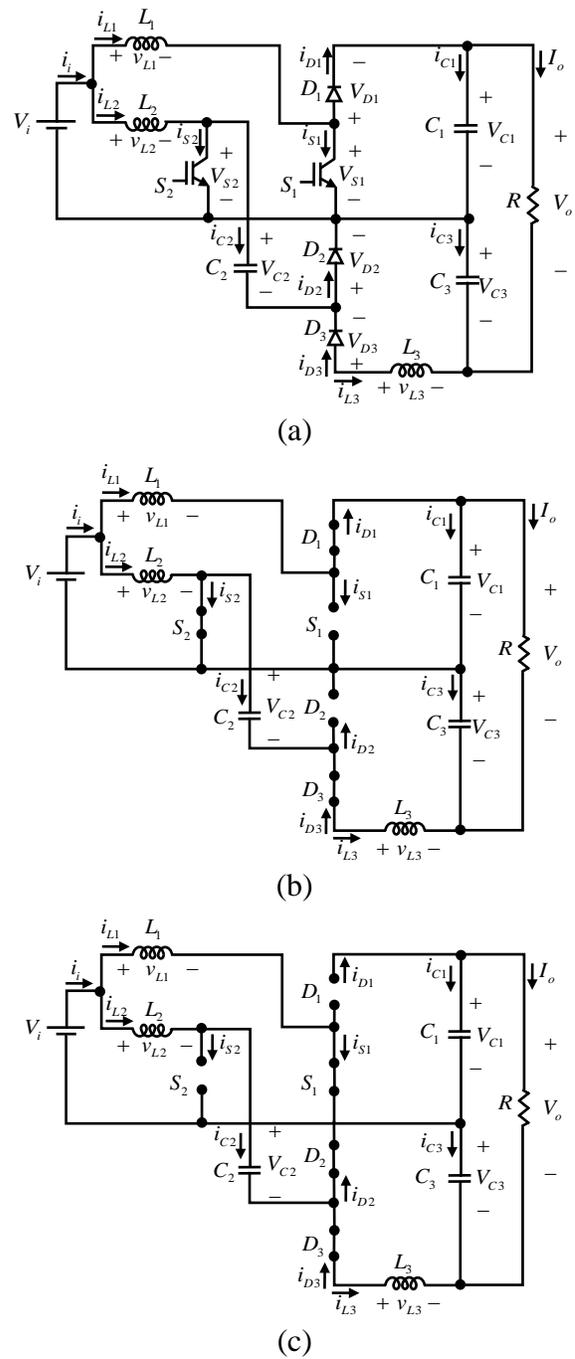


Fig.1. (a) the converter circuit provided; (b) the equivalent circuit of the converter in the time interval DT_s ; (c) the equivalent circuit of the converter provided in the time interval $(1-D)T_s$

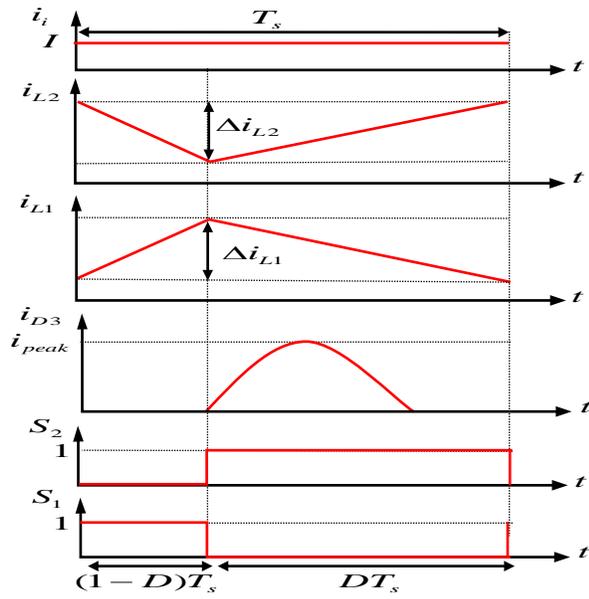


Fig. 2. shows the waveforms of the converter currents

3. Analysis of dc Characteristics of The Proposed Converter and The Elements Selection

According to fig1 the proposed converter structure is an interleaving converter type, which includes the features of an augmented converter of a high voltage transducer of three keys. In the proposed converter structure of a small inductor for finite the maximum current is used, which has no effect on the principle operation of the converter during power transmission. In addition, due to the positioning of the inductors, the current ripple in a given working cycle is zero. The number of keys has been reduced to two, and therefore the converter is controlled only by a working cycle.

3-1 Analysis of Voltage gain.

The dynamically behavior of L2 and L1 and C1, is analyzed in terms of the average

voltage and current conductivity. On the other hand, L3 , C3 and C2 has formed the form a SC circuit. However, some of the characteristics of the transducer can be obtained with the average of voltages of L2 and L1 and current of C1. With this assumption, the function of each of the keys can be replaced by its corresponding cycle of work. From now on, the converter working cycle d is defined as a percentage of the time over the whole cycle of switching time so that S2 is turned on . on the other hand can be written:

$$d = \frac{1}{T_s} \int_t^{t+T_s} q_2(\tau) d\tau \quad (1)$$

in the above relation T_s is the switching period and q_2 is The switching function of S_2 so that if the S_2 be turn on the function With this assumption and the negation of the series equivalent resistance of inductor (ESR), the average voltages of L2 and L1 are as Below:

$$L_1 \frac{di_{L1}}{dt} = d(V_i - v_{C1}) + (1-d)V_i \quad (2)$$

$$L_2 \frac{di_{L2}}{dt} = dV_i + (1-d)(V_i - v_{C2}) \quad (3)$$

In a steady state, the average voltage of the inductor must be equal to zero. Thus, the voltages of C1 and C2 in steady state are expressed as follows:

$$V_{C1} = \frac{1}{D} V_i \quad (4)$$

$$V_{C2} = \frac{1}{1-D} V_i \quad (5)$$

Therefore, the voltages of C1 and C2 can be written:

$$V_{C1} = \frac{1-D}{D} V_{C2} \quad (6)$$

$$V_{C2} = \frac{D}{1-D} V_{C1} \quad (7)$$

The dynamic currents in fig 1b are the currents of $C_1 \frac{dv_{C1}}{dt}$, di_{L1} and i_o . therefore the average current of C1 is obtained as follow:

$$C_1 \frac{dv_{C1}}{dt} = di_{L1} - \frac{v_{C1} + v_{C3}}{R} \quad (8)$$

in the steady state the average current of C1 is Equal to zero, so the average current of the L1 is as follow:

$$I_{L1} = \frac{1}{D} \left(\frac{V_{C1} + V_{C3}}{R} \right) \quad (9)$$

The C3 and C2 form SC circuit, so the dynamic behavioral equations do not apply to them. However in the steady state the L2 current can be written as below with the input and output power balancing condition according to the fig 1a:

$$I_{L2} = \frac{1}{1-D} \left(\frac{V_{C1} + V_{C3}}{R} \right) \quad (10)$$

In addition, from the fig 1a, the output voltage is as follows:

$$V_o = V_{C1} + V_{C3} \quad (11)$$

The gain of the converter supplied voltage is obtained as follows

$$\frac{V_o}{V_i} = \frac{1}{D(1-D)} \quad (12)$$

The C2 and C3 operate as a SC circuit. Because the C2 cuts off the C3 voltage as long as the S3 is turn on. this is due to the

fact that the saved energy in the L3 can be ignored compared with other elements of converter that can stored energy. In addition, in the steady-state mode the voltages of C3 and C2 are equal .

$$V_{C3} = V_{C2} \quad (13)$$

The obtained voltage gain in (12) is for ideal elements, because ESR inductors have been ignored. In practical, the leakage resistance of the inductors is limited more voltage gain, so it can be written:

$$I_{L1} = \left(1 + \frac{D}{1-D} \right) \frac{1}{D} \frac{V_{C1}}{R} = \frac{1}{D(1-D)} \frac{V_{C1}}{R} \quad (14)$$

$$I_{L2} = \left(1 + \frac{1-D}{D} \right) \frac{1}{1-D} \frac{V_{C2}}{R} = \frac{1}{D(1-D)} \frac{V_{C2}}{R} \quad (15)$$

With consideration ESR of L1 the (2) Can be expressed as following:

$$L_1 \frac{di_{L1}}{dt} = d(v_i - R_{L1}i_{L1} - v_{C1}) + (1-d)(v_i - R_{L1}i_{L1}) \quad (16)$$

in the above relationship R1 represents the ESR of L1(Not ideal). Since in the steady state the average voltage of the L1 inductors must be zero, it can be written:

$$0 = D(V_i - R_{L1}I_{L1} - V_{C1}) + (1-D)(V_i - R_{L1}I_{L1}) \quad (17)$$

$$= V_i - R_{L1}I_{L1} - DV_{C1}$$

The ratio of voltage of C1 to output voltage is as follows:

$$\frac{V_{C1}}{V_i} = \frac{1}{D + \frac{R_{L1}}{D(1-D)}R} \quad (18)$$

similarly, Considering the ESR for L2, equation 3 is written as below:

$$L_2 \frac{di_{L2}}{dt} = d(V_i - R_{L2}i_{L2}) + (1-d)(V_i - R_{L2}i_{L2} - v_{C2}) \quad (19)$$

Where, the equation in steady mode is as follows:

$$0 = D(V_i - R_{L2}I_{L2}) + (1-D)(V_i - R_{L2}I_{L2} - V_{C2}) \quad (20)$$

$$= V_i - R_{L2}I_{L2} - (1-D)V_{C2}$$

In addition, the relationship between the voltage of the C2 and the input voltage is obtained as follows:

$$\frac{V_{C2}}{V_i} = \frac{1}{(1-D) + \frac{R_{L2}}{D(1-D)R}} \quad (21)$$

Finally, the practical gain of converting is as follows:

$$\frac{V_o}{V_i} = \frac{\frac{V_i}{D + \frac{R_{L1}}{D(1-D)R}} + \frac{V_i}{(1-D) + \frac{R_{L2}}{D(1-D)R}}}{V_i} \quad (22)$$

ESR becomes smaller, by making a small inductive coil. as previously stated, the structure presented in this paper is used by inductors to reject the input current ripple in a specific working cycle. For example, if be $L_2 = 3L_1$, the input current in working cycle of $D = 75\%$ is without any ripple. It can be assumed that the ESR of inductors are equal to the inductance ratio, that is $R_{L2} = 3R_{L1}$. Under this assumption, the fig.3. shows the voltage Gain of the converter for different values of the ratio between load resistance R and R_{L2} consists of $R_{L2}/R = 0$, $R_{L2}/R = 0.0005$, $R_{L2}/R = 0.0001$, $R_{L2}/R = 0.0015$ and $R_{L2}/R = 0.002$.

According to (2), it can be seen that by increasing the ratio of R_{L2}/R the voltage gain decreases. The figure is drawn by using the relationship (22). according to the fig 3,

the minimum voltage gain occurs at 4 volts in $D = 50\%$. if the working cycle is selected less than 50%, the voltage gain increases again, resulting the converter minimum gain is about 4. the interval of $D > 50\%$ for working cycle was selected to ensure enough time of charge and discharge for L3. as a result, in order to reject the input current ripple the inductors must be selected according to $L_2 > L_1$. in addition, $L_2 > L_1$ express that must be $R_{L2} > R_{L1}$. therefore, higher voltage gains are obtained for $D < 10\%$ according to fig 3. this is a matter of compromise between the elimination of the input current ripple and the higher voltage gain. in practical applications, the dc-dc converters operate for working cycles in range $20\% < D < 80\%$. It is observed from fig.3 that in this range the voltage gain is practically symmetrical and, as a result, the voltage gain loss is the lowest value. for the working cycle $D > 50\%$, the SC circuit of converter work contains a larger power of the Transitional Power.

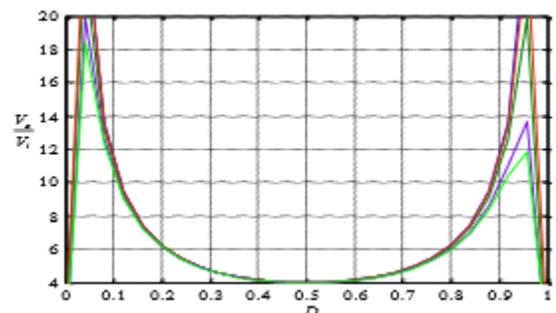


Fig .3. The voltage gain versus to the working cycle with the ESR of inductors

Fig.3 shows that ESR of inductors reduces the effective voltage gain in DC-DC converters. the presented structure at a higher switching frequency Will perform

better due to the small size of reactive elements (ESRs).

3-2 Designing of the inductor energy saver

according to the fig.1.a the Ripple of L1 and L2 energies are as follows:

$$\Delta i_{L1} = \frac{V_i (1-D)}{L_1 f_s} \quad (23)$$

$$\Delta i_{L2} = \frac{V_i D}{L_2 f_s} \quad (24)$$

Where, $F_s = 1/T_s$ is the switching frequency of the converter. The difference of inductors current Ripple is obtained from the following equation:

$$\Delta i_i = \frac{V_i}{f_s} \left(\frac{D}{L_2} - \frac{1-D}{L_1} \right) \quad (25)$$

depending on the relationship (25) the condition of zero input current Ripple is obtain of to be zero of the left side of the above equation is:

$$L_2 = L_1 \frac{D}{1-D} \quad (26)$$

If the input and output voltages are expected to be such that the work cycle by measuring $L_1 = 3L_2$ is equal to 75%, then the input current ripple deleted. already the value of L1 and L2 were selected. according to the above relation, for example, with choosing of $L_1 = 3L_2$ the relation (25) is written as follows:

$$\Delta i_i = \frac{V_i}{f_s L_1} \left(\frac{4}{3} D - 1 \right) \quad (27)$$

According to the (27), the converter eliminates the input current ripple in the of 0.75 working cycle.

3-3 Design of the maximum current limiter for inductor

As it mentioned, D3 , C2 and C3 are connect together in parallel form,because of it a inductor is necessary to limit the maximum current . however, it may not be appropriate the shape of D3 current, so it must controlled. when the S2 is switched on according to fig.1.a, the voltages of C2 and C3 are exactly equal due to their parallel connection. this voltage is shown with $V_{C,o}$.

After the S2 goes to off mode, the converter circuit is represented in the fig.1.b as result C2 and C3 does not interconnect. as long as the S2 be off at the time interval $(1-D)T_s$, the C3 is discharge via the load current. in this state, C2 is charged by the current of L2.

$V_{C2,i}$ and $V_{C3,i}$ are the final voltages of C2 and C3 that these voltages can be expressed as below:

$$V_{C2,i} = V_{C,o} + \Delta V_{C2} = V_{C,o} + \frac{I_{L2}}{C_2} (1-D)T_s \quad (28)$$

$$V_{C3,i} = V_{C,o} + \Delta v_{C3} = V_{C,o} - \frac{I_o}{C_3} (1-D)T_s \quad (29)$$

The differences of C2 and C3 voltages are as following:

$$V_{diff} = \Delta v_{C2} + \Delta v_{C3} = \left(\frac{I_{L2}}{C_2} - \frac{I_o}{C_3} \right) (1-D)T_s \quad (30)$$

If no inductor is serially with diode D_3 , the maximum current will be equal to the voltage division V_{diff} (several volts) on the resistance of this loop. The resistance of the loop is equal to the resistance of the S_2 and the D_3 and the ESR property for capacitors C2 and C3 are several millimeters. Fig. 4 shows the circuit of the current loop. If the

current exceeds the maximum current of the elements, the insertion of the inductor in the circuit is required. Fig. 5 shows that this current increases rapidly and may damage the power semiconductors if the inductor L_3 is not correctly designed. It is clear from Fig. 4 that C_{eq} is equivalent to C2 and C3. Since the inductor L_3 stores a small amount of energy, the inductor L_3 fully charges and discharges in a switching cycle and smoothes the capacitor current. But the inductor L_3 produces a resonant impedance peak at a resonant frequency. Given the equivalent circuit of fig.4, the resonance frequency is obtained from the following equation:

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{L_3 C_{eq}}} \quad (31)$$

As explained, the converter will be used in a work cycle larger than 50%. Therefore, the L_3 must be chosen to be $f_o > f_s$. This condition ensures that the L_3 will be fully deactivated before the start of the next switching step for all values of the work cycle in a range of functions, and will determine the basis for eliminating the maximum current within the loop. At the beginning of the charging mode, the current begins to increase with a slope equal to $i_{L3} = (V_{diff} / L_3)t$. Hence, the current of the loop, since $i_{L3} = \hat{i}_{L3} \sin(\omega_o t)$, and its derivative in $t=0$ can be calculated, is assumed to be $\frac{V_{diff}}{L_3}$. The value of \hat{i}_{L3} is obtained as follows:

$$\hat{i}_{L3} = \frac{V_{diff}}{\omega_o L_{d3}} \quad (32)$$

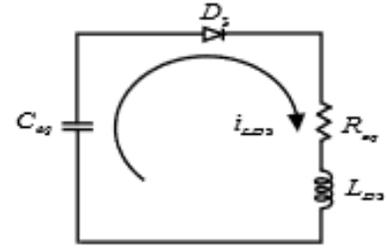


Fig.4. The Circuit of current loop in the proposed converter

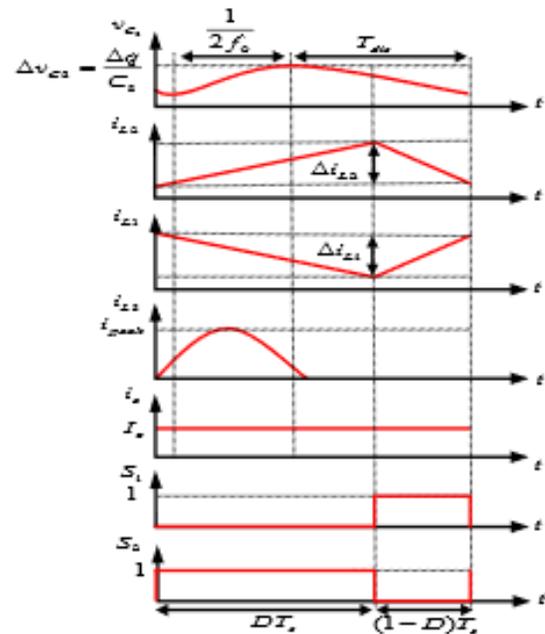


Fig.5. Waveforms for selecting the reactive element

3-4 The design of the capacitor

As long as the S_1 is on, for the time interval $(1-D)T_s$ the current of the C1 is obtained as follows:

$$\Delta V_{C1} = -\frac{I_o}{C_1}(1-D)T_s \quad (33)$$

When the S_1 is on, for time interval $(1-D)T_s$, the charge C2 is charged on the current through the inductor L_2 , so it can be written:

$$\Delta V_{C_2} = \frac{I_{L_2}}{C_2}(1-D)T_s \quad (34)$$

The C_3 is chosen based on the fact that the L_3 is the average current equal to the load current. When the instantaneous current of this inductance exceeds the current, the C3 starts charging, and as a result, the voltage of the two ends increases to ΔV_{C_3} as given by $\Delta q/C_3$. This is shown in fig. 5, where the shadowy area shows charge Δq . After the L_3 has been selected, according to Fig. 5, the time taken for charging the C3 can be obtained by finding when $i_o < i_{L_3}$ occurs. Then, the C3 is discharged at the other keying time. The increase in the voltage of the C3 is:

$$T_{dis} = T_s - \left[\frac{1}{2f_o} - \frac{2}{\omega_o} \arcsin \left(\frac{i_o}{\hat{i}_{L_3}} \right) \right] \quad (35)$$

In the above relation T_{dis} is equal to the discharge time of the C3. Since, during this period, C3 follows the load current, it can be written:

$$\Delta V_{C_3} = \frac{I_o}{C_3} T_{dis} \quad (36)$$

Which, Makes it possible to measure and estimates Of C3.

4. Simulation Results

The proposed power converter circuit used for simulation is shown in Fig. 1.a. Table (1) shows the list of elements used to simulate

the proposed converter. Given the relation (26) for the values given for the L1 and L2 in Table1, the zero input current ripple mode is created for the converter operation in the $D = 0.7$ cycle. The value of the L3, as already stated, should be such that the large refresh rate of the switching frequency is confirmed in the S1 switching mode, and it has already been stated that its size can be approximately 1/100 of the size of L2 or about 1/50 of the L1.

Accordingly, the value of the L3 can be considered by trial and error $L_3 = 6^{th}$. The ON resistance of the keys and diodes is considered to be small and equal to 0.001Ω and ideal. In this way, the simulation results will be confirmed using relations that the ESR does not consider the elements. Fig.6 shows the simulation results of the proposed converter for the $D = 0.7$ cycle. With respect to the figure, it can be seen that the ripple of input current is zero (approximately 0.08^A or 1.29%).

The simulation results obtained in this section have already been proven analytically. In accordance with equation 12, for the working cycle $D = 0.7$, with the input voltage V_i being determined from table (1), the value obtained for the output voltage is equal to $V_o = 71.4V$ and corresponds to the value obtained from the simulation. With reference to (4) and with the determination of the input voltage V_i of Table (4-1), we can obtain the voltages of C1 and C2, respectively, equal to $V_{C_1} = 21.4V$ and $V_{C_2} = 50V$, the results shown in fig. 6, also Confirm the values.

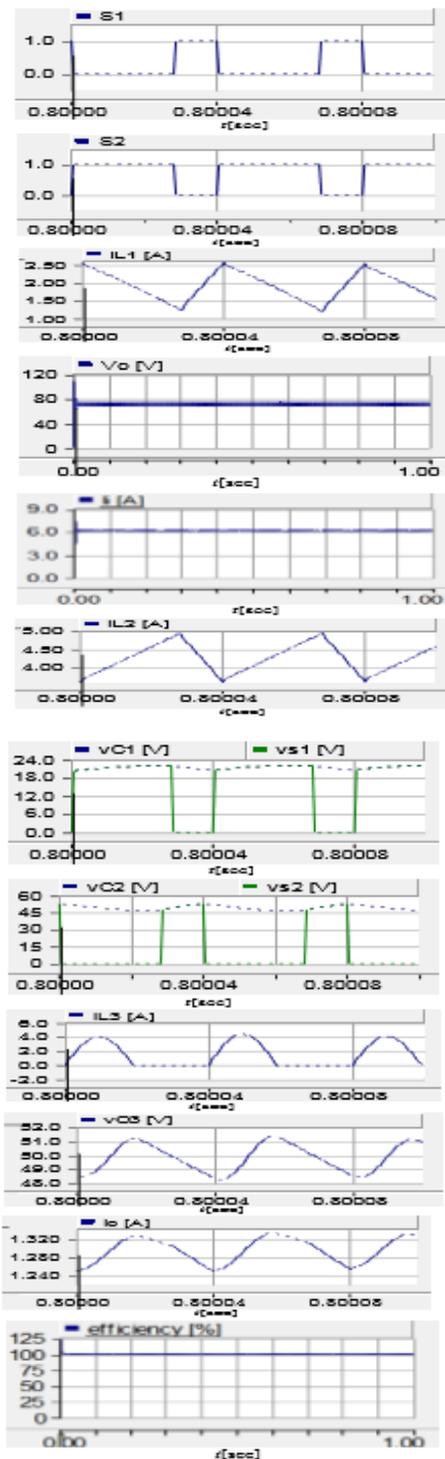


Fig.6.The waveforms of the voltage and current for proposed converter for the working cycle $D = 0.70$

Table.1.List of elements used for simulation.

Power dc voltage input	15v
Output dc voltage	71v
Inductor L_3	$L_3=6 \text{ uH}$
Inductor L_2	330 uH
Inductor L_1	140 uH
Capacitor $C_1=C_2=C_3$	10 uF
Duty cycle D	$D=0.7$
Output resistor R_O	55Ω
Cut off frequency f_s	25 kHz

According to equation 13, it is observed that the steady-state voltage of the C2 and C3 are equal and this is shown in Fig. 6. The efficiency obtained for simulating the converter's performance in the working cycle $D = 0.7$ is 99.96% , as shown in Fig. 6. For a working cycle $D = 0.65$, the size of the L2 is the same as given in Table (1), but the size of the L1 must be chosen according to relation (26) to be equal to $177.69^{\mu H}$ so that the zero mode of the input current for the converter function is created in the working cycle $D = 0.65$. The size of the other elements used for the working cycle $D = 0.65$ is the same as the elements specified in table.1. For this purpose, the simulation results will be confirmed using relationships that have not been considered by the ESR. Figure 7 shows the simulation results of the proposed converter for the working cycle $D = 0.65$.

According to this figure, it can be seen that the ripple of input current is approximately zero. The simulation results obtained in this section have already been proven analytically. In accordance with equation 12 , for the working cycle $D = 0.65$, with the input voltage V_i being determined

from table.1, the value obtained for the output voltage is equal to $V_o = 65.93V$ and corresponds to the value obtained from the simulation. With reference to (4) and with the determination of the input voltage V_i of Table.1, we can obtain the C1 and C2 voltages $V_{C1} = 23.07V$ and $V_{C2} = 42.85V$ respectively, the results shown in fig. 7 also give these values they confirm. According to Equation13, it is observed that the steady-state voltage of the C2 and C3 are equal, and this is shown in fig. 7. The efficiency obtained for simulating the converter's performance in the working cycle $D = 0.65$ is equal to 99.96% as shown in fig. 7.

5. Conclusion

In this paper, the structure of a new dc-dc converter structure is presented by removing the ripple of the input current in a desired work cycle, and this capability is obtained without increasing the number of elements. In addition, the converter produces a high voltage gain without the need for large amounts of working cycles or incremental transformers. These characteristics make the converter suitable for transferring electrical power of low voltage sources such as renewable sources . Hence, the presented structure here offers many benefits, unlike transformer or pre-coupling structures. Also, the validity of the obtained structure relationships was implemented in PSCAD software and simulation results were presented. The results of the simulations confirm the validity of the obtained results and the obtained relationships for the proposed structure.

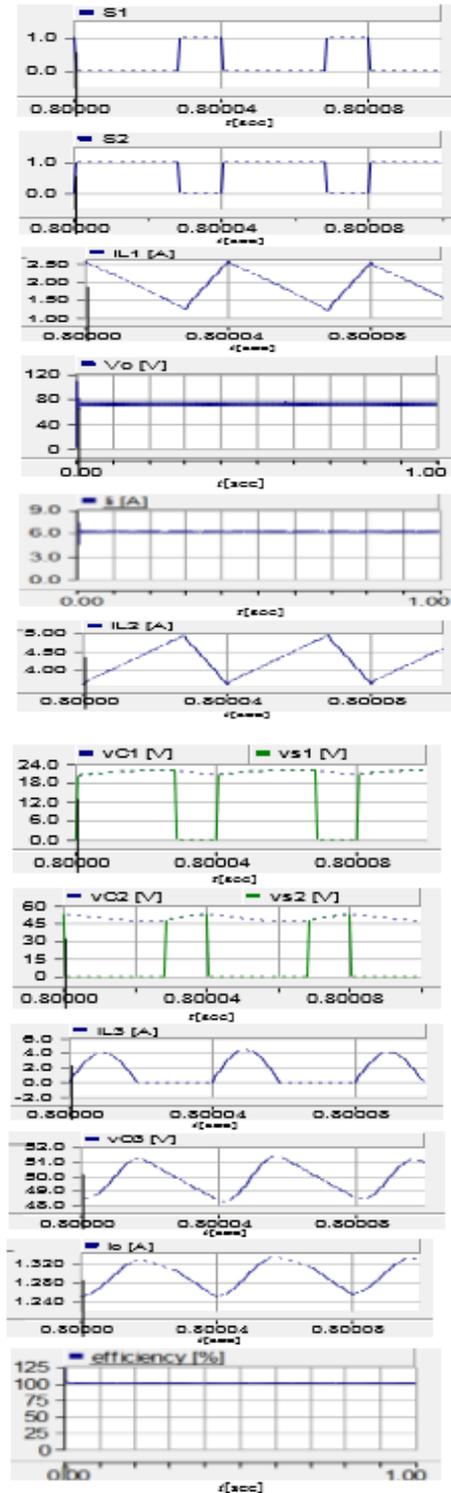


Fig.7.The waveforms of the voltage and current for proposed converter for the working cycle

$$D = 0.65$$

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